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OSCI TLM Working Group Status

by

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Presentation Overview

- Progression of OSCI TLM standards
- Current OSCI TLM WG roster
- TLM 2.0 work-in-progress
- TLM 2.0 draft 2 public review
- TLM 2.0 draft 2 feedback
- TLM 2.0 schedule
- TLM standards roadmap
- Summary

Progression of OSCI TLM Standards

TLM-2005-04-08 TLM 1.0	TLM-2006-11-29 TLM 2.0 draft 1	2007-06-27 TLM 2 requirements, glossary, whitepaper	TLM-2007-11-29 TLM 2.0 draft 2
•bidirectional I/F ▪"transport" ▪blocking •uni-directional I/F ▪"FIFO-like" ▪blocking ▪non-blocking (effective pass-by-value; split request/ response)	•TLM 1.0 •timing annotation of TLM 1.0 I/Fs •standard payload ▪extension •analysis port (effective pass-by-value; split request/ response)	•TLM 1.0 (legacy) •coding styles ▪untimed ▪loosely-timed ▪approx-timed** •layered solution ▪generic technology ▪MMB-specifics •temporal decoupling •debug transactions* •direct memory** •model sync** •endianness •standard payload* ▪extension* •analysis port	•satisfies all requirements •payload event queue •quantum keeper •users manual •training presentation (pass-by-reference; whole transaction)

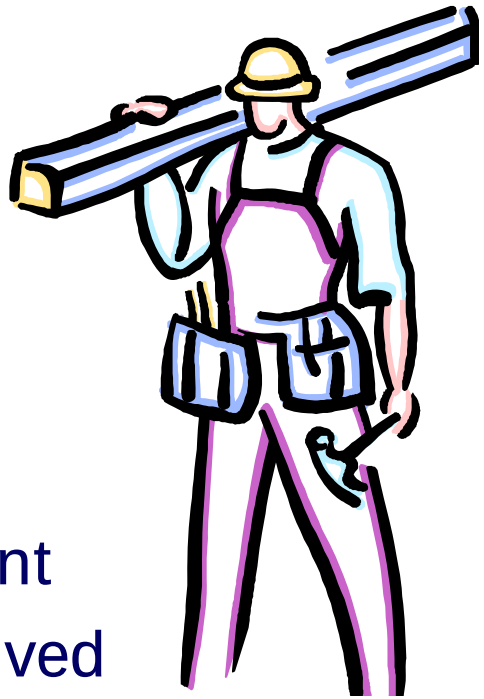
* improved, ** stretch

Current OSCI TLM WG Roster

- 106 individuals from 25 organizations
- ~19 individuals from ~15 organizations participate regularly in weekly 2-hour teleconference

TLM 2.0 Work-In-Progress

- Refinements and improvements being investigated since the release of draft 2
  - Simplifying endianness
  - DMI extensions
  - PEQ consistency
  - Locking & atomic transactions
  - Analysis ports – assess overall value
  - Generic payload mutability enforcement
- It is unlikely that all of these will be resolved for TLM 2.0



TLM 2.0 draft 2 Public Review

- 905 downloads of the draft 2 kit (as of 1/10/08)
- Feedback received from ARM, Cadence, CoWare, Doulos, ECSI (1/29 TLM-2 Workshop), Emulex, ESLX, Freescale, Fujitsu, GreenSocs, Infineon, JEITA, NXP, ST, STARC, SPRINT, Thomson, Virtutech
- Overall, feedback is supportive and encouraging
- Significant requests and suggestions for improvement
  - The TLM WG will be diligent in thoroughly reviewing and addressing all of these requests
  - Some are contradictory (e.g. “add locking support” and “do not add locking support”); can’t please everyone

TLM 2.0 draft 2 Feedback

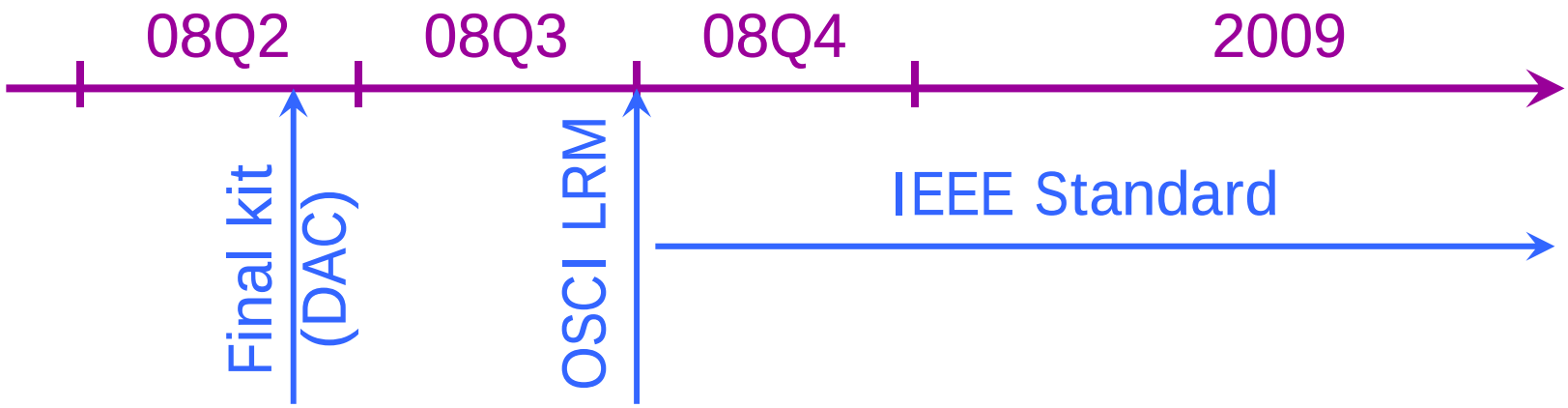
- Summary of specific feedback is appended; categories are:
  - General
  - tlm_generic_payload
  - b_transport
  - nb_transport
  - Sockets
  - Direct Memory Interface
  - Temporal Decoupling
  - Tlm_quantumkeeper
  - Debug Transaction I/F
  - Users Manual
  - Payload Event Queue
  - Examples
  - Code
  - Build Environment
  - *Outside OSCI scope*
  - *TLM roadmap items*
  - *Issues already resolved*

TLM 2.0 schedule

Deploy for production use
(TLM 2.0 OSCI LRM)

Adapt methods, tools & flows
(final TLM 2.0 kit)

Start training and consulting now (draft 2)



TLM Standards Roadmap

- Areas to standardize after TLM 2.0 (order not yet determined)
  - Analysis (beyond analysis port) & visibility
  - Configuration
  - Control
  - Cycle-accurate modeling
  - Debug (beyond debug transaction)
    - Hardware watchpoints
  - Registers
  - TLM 2.0 WIP items not completed

Summary

- TLM interoperability standards are a reality in 2008!
- Draft 2 is closing in on the target; focus is now on addressing feedback
  - Thanks to those who provided feedback!
- There's (always) more to do
  - OSCI LRM
  - IEEE Standard
  - Expanding the TLM standard (e.g. TLM 2.1 & beyond)
- Get involved by joining OSCI
  - More influence
  - Accelerate standards